	L #	Hits	Search Text	DBs	Time Stamp
1	L1	20202	getter$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07
2	L2	3719448	plug or contact	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07
3	L3	353619	dop$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07
4	L4	580837	dop$6 or implant$6 or inplant$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07

	L #	Hits	Search Text	DBs	Time Stamp
5	L5	1850	getter$6 same dop$6 same (dop$6 or implant$6 or inplant$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07
6	L6	14584781	phosphorous or P or arsenic or ar or antimony or sb or bismuth or bi or boron or B or aluminium or Al or gallium or Ga or indium or In or helium or He or neon or Ne or argon or ar or krypton or kr or xenon or Xe or germanium or Ge	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07
7	L7	1415	(getter$6 same dop$6 same (dop$6 or implant$6 or inplant$6)) same (phosphorous or P or arsenic or ar or antimony or sb or bismuth or bi or boron or B or aluminium or Al or gallium or Ga or indium or In or helium or He or neon or Ne or argon or ar or krypton or kr or xenon or Xe or germanium or Ge)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07
8	L9	4505634	plug or contact or groove or trench$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07

	L #	Hits	Search Text	DBs	Time Stamp
9	L10	846	getter$6 near4 (plug or contact or groove or trench$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07
10	L8	55	getter$6 near8 (plug or contact) near8 (dop$6 or implant$6 or inplant$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07
11	L13	56	((getter$6 near4 (plug or contact or groove or trench$3)) near8 (phosphorous or P or arsenic or ar or antimony or sb or bismuth or bi or boron or B or aluminium or Al or gallium or Ga or indium or In or helium or He or neon or Ne or argon or ar or krypton or kr or xenon or Xe or germanium or Ge)) not (((getter$6 near4 (plug or contact or groove or trench$3)) near8 (phosphorous or P or arsenic or ar or antimony or sb or bismuth or bi or boron or B or aluminium or Al or gallium or Ga or indium or In or helium or He or neon or Ne or argon or ar or krypton or kr or xenon or Xe or germanium or Ge)) and (@ad<"20010403"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07

	L #	Hits	Search Text	DBs	Time Stamp
12	L14	60	getter$6 near8 (plug or contact or groove or trench$3) near8 (doped or doping or implant ot implanting)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07
13	L15	2	("6095008").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07
14	L12	156	((getter$6 near4 (plug or contact or groove or trench$3)) near8 (phosphorous or P or arsenic or ar or antimony or sb or bismuth or bi or boron or B or aluminium or Al or gallium or Ga or indium or In or helium or He or neon or Ne or argon or ar or krypton or kr or xenon or Xe or germanium or Ge)) and (@ad<"20010403")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07

	L #	Hits	Search Text	DBs	Time Stamp
15	L11	212	(getter$6 near4 (plug or contact or groove or trench$3)) near8 (phosphorous or P or arsenic or ar or antimony or sb or bismuth or bi or boron or B or aluminium or Al or gallium or Ga or indium or In or helium or He or neon or Ne or argon or ar or krypton or kr or xenon or Xe or germanium or Ge)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:07
16	L16	1154	((438/310) or (438/311) or (438/143) or (438/402) or (438/471) or (438/473) or (438/517)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:10
17	L17	51	16 and 10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:10

	L #	Hits	Search Text	DBs	Time Stamp
18	L18	39	17 and ((@ad<"20010403") or (@rlad<"20010403"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:11
19	L19	30	18 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/02 07:12

US-PAT-NO: 6586295

DOCUMENT-IDENTIFIER: US 6586295 B2

TITLE: Semiconductor device manufacturing method and semiconductor device

---------- KWIC ---------

Abstract Text - ABTX (1):

A trench 5 for element separation is formed in a silicon substrate 1 by an etching process using an SiO.sub.2 film 2 as a mask (FIG. 1B). Side walls 18 are formed in a manner covering the trench 5 laterally (FIG. 1C). Defect-forming ions such as silicon ions are **implanted** into the silicon substrate 1 with the SiO.sub.2 film 2 and side walls 18 used as a mask, whereby a gettering layer 1 is formed only at a bottom of the trench 5.

Application Filing Date - AD (1):

20010108

Brief Summary Text - BSTX (6):

In the field of semiconductor devices, there is a known technique for removing from a silicon substrate defects and metal impurities that may adversely affect device characteristics. That technique involves intentionally forming a defective layer (called a gettering layer) in internal regions of the silicon substrate in such a manner that the formed layer will capture those defects and metal impurities from within the substrate. The gettering layer may be fabricated illustratively by **implanting** oxygen or silicon ions into the silicon substrate.

Brief Summary Text - BSTX (7):

FIGS. 11A through 11D and 12A through 12C show a flow of conventional processes in which a gettering layer is formed by **implanting** ions into element isolation regions of a DRAM having a trench isolation structure. Conventionally, as indicated in FIG. 11A, an SiO.sub.2 film 2 is

first formed
by CVD on a silicon substrate 1. On the SiO.sub.2 film 2 is formed a resist
film 3 having openings where element isolation regions are to be fabricated.
After the SiO.sub.2 film 2 is etched with the resist film 3 used as a mask, the
resist film 3 is removed.

Brief Summary Text - BSTX (9):
Silicon ions are then **implanted** into the silicon substrate 1. This forms a
defective layer called a gettering layer 4 in regions close to the trench 5 in
the silicon substrate 1, as shown in FIG. 11C. The gettering layer 4 is formed
not only near the bottom of the trench 5 but also in the vicinity of its sides.

Brief Summary Text - BSTX (11):
Gate electrodes 7 are then formed on the silicon substrate 1 with a gate
insulation film interposed therebetween, as shown in FIG. 12A. When impurities
are **implanted** into the substrate using the gate electrodes 7 as a mask, source
drain impurity layers 8 and 9 are formed over the surface of the silicon
substrate 1.

Brief Summary Text - BSTX (19):
The above objects of the present invention are achieved by a method for
manufacturing a semiconductor device having a trench isolation structure. In
the method, defect-forming ions are **implanted** into a silicon substrate so as to
form a **gettering layer only at a bottom of a trench** formed in said silicon
substrate.

Brief Summary Text - BSTX (20):
The above objects of the present invention are also achieved by a method for
manufacturing a semiconductor device having a trench isolation structure. In
the method, defect-forming ions are **implanted** into a silicon substrate so as to
form a **gettering layer in regions where a trench** is to be formed in said

silicon substrate. Defective elements are captured into said gettering layer
from within said silicon substrate. The gettering layer having said defective
elements captured therein is removed during formation of said trench in said
silicon substrate.

Detailed Description Text - DETX (8):
With the SiO.sub.2 film 2 and the side walls 18 used as a mask, silicon ions
are **implanted** into an exposed bottom of the trench 5 in the silicon substrate
1. This forms a gettering layer 4 only at the bottom of the trench 5 in a
self-aligned manner, as illustrated in FIG. 1D.

Detailed Description Text - DETX (10):
Gate electrodes 7 are then formed on the silicon substrate 1 with a gate
insulation film interposed therebetween, as shown in FIG. 2B. **Implanting**
impurities using the gate electrodes 7 as a mask fabricates source drain
impurity layers 8 and 9 over the surface of the silicon substrate 1.

Detailed Description Text - DETX (13):
As described and according to the method for manufacturing the semiconductor
device as the first embodiment, the gettering layer 4 is formed in a
self-aligned manner only at the bottom of the trench 5 with no defective layer
formed near the side walls of the trench 5. This makes it possible to prevent
unfailingly any **contact between the gettering** layer 4 and the source drain
impurity layer 8, whereby a semiconductor device with stable characteristics is
fabricated.

Detailed Description Text - DETX (18):
With the SiO.sub.2 film 2 used as a mask, silicon ions are **implanted** into
the silicon substrate 1 as depicted in FIG. 3B. The silicon ions are **implanted**
in such a manner that they will reach regions deeper than a trench to be formed
for element isolation. As a result, a gettering layer 4 is formed deeper than
element isolation regions.

Detailed Description Text - DETX (21):
As described and according to the method for manufacturing the semiconductor device as the second embodiment, the defects stemming from **implantation** of silicon ions into the silicon substrate 1 are removed during formation of the trench 5 except for those defects that exist deeper than the trench 5. This allows the gettering region 4 to be formed only near the bottom of the trench 5. The method of the second embodiment, as with the first embodiment, permits manufacture of a semiconductor device with stable characteristics.

Detailed Description Text - DETX (22):
Although the second embodiment above was shown having ions **implanted** with the SiO.sub.2 film 2 used as a mask, as shown in FIG. 3B, this is not limitative of the invention. Alternatively, as in the case of the first embodiment, side walls 18 may be formed laterally in the openings of the SiO.sub.2 film 2 so as to perform ion **implantation** using both the SiO.sub.2 film 2 and the side walls 18 as a mask.

Detailed Description Text - DETX (28):
With the Si.sub.3 N.sub.4 film 20 and the side walls 18 used as a mask, silicon ions are **implanted** into an exposed bottom of the trench 5 in the silicon substrate 1. This forms a gettering layer 4 only at the bottom of the trench 5 as illustrated in FIG. 6A.

Detailed Description Text - DETX (37):
With the Si.sub.3 N.sub.4 film 20 and the side walls 18 used as a mask, silicon ions are **implanted** into exposed portions of the silicon substrate 1. The silicon ions are **implanted** in such a manner that they will reach regions shallower than a trench formed for element isolation. As a result, a gettering layer 4 is formed in portions where the trench is to be formed in the silicon substrate 1, as shown in FIG. 8C.

Detailed Description Text - DETX (42):
Although the fourth embodiment above was shown having ions **implanted** with both the Si.sub.3 N.sub.4 film 20 and the side walls 18 used as a mask, as shown in FIG. 8C, this is not limitative of the invention. Alternatively, ion **implantation** may be carried out with only the Si.sub.3 N.sub.4 film 20 used as the mask while the side walls 18 are excluded from assuming the role of a mask.

Detailed Description Text - DETX (44):
A method for manufacturing a semiconductor device according to a first aspect of the invention permits formation of a **gettering layer only at a bottom of a trench**. The structure unfailingly forestalls any **contact between the gettering** layer and an impurity layer formed close to the surface of a silicon substrate, whereby a semiconductor device with stable characteristics is manufactured.

Detailed Description Text - DETX (45):
One preferred method for manufacturing a semiconductor device according to the first aspect of the invention causes defect-forming ions to be **implanted** into the silicon substrate using a trench-forming mask. In this case, a gettering layer is formed in a self-aligned fashion only under the trench. This allows the desired gettering layer to be formed with precision using a simplified manufacturing procedure.

Detailed Description Text - DETX (46):
Another preferred method for manufacturing a semiconductor device according to the first aspect of the invention causes defect-forming ions to be **implanted** into a trench covered with side walls so as to form a gettering layer. This permits accurate formation of the gettering layer (i.e., defective layer) only at a bottom of the trench with no defective layer formed laterally along the trench.

Detailed Description Text - DETX (47):
A further preferred method for manufacturing a semiconductor device according to the first aspect of the invention permits fabrication of a **gettering layer in regions deeper than a trench** prior to trench formation. After formation of the **gettering layer, the trench** is fabricated so that the portions damaged by defect-forming ions are removed from the silicon substrate except for those portions to be left intact to constitute the gettering layer. This permits formation of the desired gettering layer with precision using a simplified manufacturing procedure.

Detailed Description Text - DETX (49):
A method for manufacturing a semiconductor device according to a second aspect of the invention permits formation of a **gettering layer in regions where a trench** is to be formed so that defective elements are captured into the gettering layer from with in the silicon substrate. During formation of the **trench, the gettering** layer having the defective elements captured therein is removed from the silicon substrate. This permits manufacture of a semiconductor device with stable characteristics having no defective layer close to element separation regions.

Detailed Description Text - DETX (50):
One preferred method for manufacturing a semiconductor device according to the second aspect of the invention causes defect-forming ions to be **implanted** into the silicon substrate using a trench-forming mask. In this case, a gettering layer is formed only in the regions where the trench is to be formed in a self-aligned manner. This allows the desired gettering layer to be formed with precision using a simplified manufacturing procedure.

Detailed Description Text - DETX (51):
Another preferred method for manufacturing a semiconductor device according

to the second aspect of the invention forms a gettering layer by **implanting** defect-forming ions into a trench of a first depth whose side surfaces are covered laterally with side walls. This permits precise fabrication of the gettering layer in regions deeper than the first depth with no defective layer formed laterally along the trench.

Claims Text - CLTX (1):
1. A method for manufacturing a semiconductor device having a trench isolation structure, said method comprising: forming a trench forming mask over said silicon substrate; etching said silicon substrate using said trench-forming mask so as to form a trench in said silicon substrate; forming side walls for covering laterally said trench; and **implanting** defect-forming ions into said silicon substrate using said trench-forming mask and said side walls as a mask to form a **gettering layer only at a bottom of the trench** in said silicon substrate.

Claims Text - CLTX (2):
2. A method for manufacturing a semiconductor device having a trench isolation structure, said method comprising: furnishing a trench-forming mask over said silicon substrate; **implanting** defect-forming ions, using said trench-forming mask as mask, to form a **gettering layer deeper than regions where a trench** is to be formed in said silicon substrate; and etching said silicon substrate by use of said trench-forming mask following **implantation** of said defect-forming ions, thereby forming said **trench in said silicon substrate, wherein the gettering** layer is formed only at a bottom of the trench formed in said silicon substrate.

Claims Text - CLTX (3):
3. The method for manufacturing a semiconductor device according to claim 2, further comprising the step of forming side walls for laterally covering openings in said trench-forming mask; wherein said defect-forming

ions are
implanted into said silicon substrate using said trench-forming mask and said
side walls as a mask.

Claims Text - CLTX (4):
4. A method for manufacturing a semiconductor device having a trench
isolation structure, said method comprising the steps of: **implanting** defect-forming ions into a silicon substrate so as to form a **gettering layer in
regions where a trench** is to be formed in said silicon substrate; capturing
defective elements into said gettering layer from within said silicon substrate; and removing said gettering layer having said defective elements
captured therein during formation of said trench in said silicon substrate.

Claims Text - CLTX (5):
5. The method for manufacturing a semiconductor device according to claim
4, further comprising the step of furnishing a trench-forming mask over said
silicon substrate; wherein said defect-forming ions are **implanted,** using said
trench-forming mask as a mask, into the regions where said trench is to be
formed in said silicon substrate.

Claims Text - CLTX (6):
6. The method for manufacturing a semiconductor device according to claim
5, wherein said step of forming said gettering layer further comprises the
steps of: etching said silicon substrate using said trench-forming mask so as
to form a trench having a first depth in said silicon substrate; forming side
walls for covering laterally said trench having said first depth; and
implanting said defect-forming ions into said silicon substrate using said
trench-forming mask and said side walls as a mask so as to form a **gettering
layer at a bottom of said trench** having said first depth; and wherein said
step of removing said **gettering layer further comprises the step of etching
said trench** having said first depth down to a second depth in order

to remove
said gettering layer having said defective elements captured therein.

Claims Text - CLTX (7):
7. The method for manufacturing a semiconductor device according to claim
5, further comprising the step of forming side walls for covering laterally
openings of said trench-forming mask; wherein said defect-forming ions are
implanted into said silicon substrate using said trench-forming mask and said
side walls as a mask.

Current US Cross Reference Classification - CCXR (4):
438/473